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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,630	10/27/2003	Shih-Hsiung Lin	JCLA9730	5386

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,630	LIN ET AL.	
	Examiner	**Art Unit**	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *75-101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *75-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Serial Number: 10/695630 Attorney's Docket #: MEGP0005USA4
Filing Date: 10/27/2003; claimed foreign priority to 10/25/2002

Applicant: Lin et al.

Examiner: Alexander Williams

Applicant's election of the sub-species II, figure 45, claims 75-101 filed 10/28/05, has been acknowledged.

Claims 1-74 have been cancelled.

]

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: Applicant's related application information should be updated.

Appropriate correction is required.

The drawings are objected to because in figure 45, the item "790" is not described in the specification.

Correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the trace over said passivation layer, and a second pad over said passivation layer, wherein said second pad is connected to said first pad through said trace and has a position different from that of said first pad from a top view in claim 94 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 94 to 101 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 94, it is unclear and confusing to what is meant by "a trace over said passivation layer, and a second pad over said passivation layer, wherein said second pad is connected to said first pad through said trace and has a position different from that of said first pad from a top view." Which is this shown in the drawing of the elected species?

Any of claims 94 to101 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 75 to 79, 81 to 90 and 92 to 100, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuo et al. (U.S. Patent # 6,787,442 B2).

75. Hayashida et al. (figures 1 to 30) specifically figures 3 and 6 show a multi-chip structure comprising: a first chip **9**; a second chip **11**; a conductive pillar **6** on the first chip, wherein said conductive pillar has a height greater than 3 microns; and a tin-containing material **8** connecting said conductive pillar to said second chip.

76. The structure of Claim 75, Hayashida et al. show wherein said conductive pillar comprises copper.

77. The structure of Claim 75, Hayashida et al. show wherein said conductive pillar comprises nickel.

78. The structure of Claim 75, Hayashida et al. show wherein said conductive pillar comprises gold.

79. The structure of Claim 75, Hayashida et al. show wherein said conductive pillar comprises tin.

81. The structure of Claim 75, Hayashida et al. show wherein said tin-containing material further comprises lead.

82. The structure of Claim 75, Hayashida et al. show wherein said tin-containing material further comprises silver.

83. Hayashida et al. (figures 1 to 30) specifically figures 3 and 6 show a multi-chip structure, comprising: a first chip **9** comprising: a semiconductor substrate comprising multiple MOS devices, an interconnection layer **15c-e** over said semiconductor

substrate, a first pad **9a** over said semiconductor substrate, a passivation layer **15j** over said interconnection layer, an opening in said passivation layer exposing said first pad, and a second pad **15f** over said passivation layer, wherein said second pad is connected to said first pad and has a position different from that of said first pad from a top view; a conductive pillar **6** on said second pad, wherein said conductive pillar has a height greater than 3 microns; a second chip **11** over said first chip; and a tin-containing material **8** connecting said conductive pillar to said second chip.

84. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises copper.

85. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises nickel. 5

86. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises gold.

87. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises tin.

88. The structure of Claim 83, Hayashida et al. show wherein said second pad comprises gold.

89. The structure of Claim 83, Hayashida et al. show wherein said second pad comprises an electroplated

90. The structure of Claim 83, Hayashida et al. show wherein said second has a thickness greater than 1 micron.

92. The structure of Claim 83, Hayashida et al. show wherein said tin-containing material further comprises lead.

93. The structure of Claim 83, Hayashida et al. show wherein said tin-containing material further comprises silver.

94. Hayashida et al. (figures 1 to 30) specifically figures 3 and 6 show a multi-chip structure, comprising: a first chip **9** comprising: a semiconductor substrate comprising multiple MOS devices, an interconnection layer **15c** over said semiconductor substrate, a first pad **9a** over said semiconductor substrate, a passivation layer **15j** over said interconnection layer, an opening in said passivation layer exposing said first pad, a

trace **15d-e** over said passivation layer, and a second pad **15f** over said passivation layer, wherein said second pad is connected to said first pad through said trace and has a position different from that of said first pad from a top view; a second chip **11** over said first chip; and a bump **6** connecting said second pad to said second chip.

95. The structure of Claim 94, Hayashida et al. show wherein said bump comprises copper.

96. The structure of Claim 94, Hayashida et al. show wherein said bump comprises nickel.

97. The structure of Claim 94, Hayashida et al. show wherein said bump comprises gold.

98. The structure of Claim 94, Hayashida et al. show wherein said bump comprises tin.

99. The structure of Claim 94, Hayashida et al. show wherein said bump comprises lead.

100. The structure of Claim 94, Hayashida et al. show wherein said bump comprises silver.

(62) When the multi-chip module having a structure as illustrated in FIG. 3 is packaged in the form as illustrated in FIG. 8, a large stress is applied to the boundary portion between the solder bumps 6 or solder external electrodes 18 and the corresponding underlying second conductor films (Ni films 4, Ni films 13c), because there is a large difference in the thermal expansion coefficient between the semiconductor chip 9 and the module substrate 11 or mother board 13 upon solder reflow for mounting thereon the solder bumps 6 or solder external electrodes 18; each semiconductor chip 9 is fixed to the module substrate 11 with the adhesive material 19; and the Sn/Ni alloy layer 8 is formed between each of the solder bumps 6 and each of the second conductor films (Ni films 4, Ni films 13c). Soldering as illustrated in FIG. 1, however, improves solder bonding property, thereby making it possible to prevent peeling of the solder bumps 6 or solder external electrodes 18.

Claims 75 to 101, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Matsuo et al. (U.S. Patent Application Publication # 2003/0052409 A1).

75. Matsuo et al. (figures 1 to 19) specifically figures 1 and 12 show a multi-chip structure comprising: a first chip **10, 303**; a second chip **308**; a conductive pillar **304,308** on the first chip, wherein said conductive pillar has a height greater than 3 microns; and a tin-containing material connecting said conductive pillar to said second chip.

76. The structure of Claim 75, Matsuo et al. show wherein said conductive pillar comprises copper.

77. The structure of Claim 75, Matsuo et al. show wherein said conductive pillar comprises nickel.

78. The structure of Claim 75, Matsuo et al. show wherein said conductive pillar comprises gold.

79. The structure of Claim 75, Hayashida et al. show wherein said conductive pillar comprises tin.

80. The structure of Claim 75, Hayashida et al. further comprising a wire formed by a wirebonding process and connected to said first chip.

81. The structure of Claim 75, Hayashida et al. show wherein said tin-containing material further comprises lead.

82. The structure of Claim 75, Hayashida et al. show wherein said tin-containing material further comprises silver.

83. Matsuo et al. (figures 1 to 19) specifically figures 1 and 12 show a multi-chip structure, comprising: a first chip **1,303** comprising: a semiconductor substrate **10** comprising multiple MOS devices, an interconnection layer **14** over said semiconductor substrate, a first pad **12C** over said semiconductor substrate, a passivation layer **15** over said interconnection layer, an opening in said passivation layer exposing said first pad, and a second pad **18,20** over said passivation layer, wherein said second pad is connected to said first pad and has a position different from that of said first pad from a top view; a conductive pillar **21** on said second pad, wherein said conductive pillar has a height greater than 3 microns; a second chip **307** over said first chip; and a tin-containing material connecting said conductive pillar to said second chip.

84. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises copper.

85. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises nickel.

86. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises gold.

87. The structure of Claim 83, Hayashida et al. show wherein said conductive pillar comprises tin.

88. The structure of Claim 83, Hayashida et al. show wherein said second pad comprises gold.

89. The structure of Claim 83, Hayashida et al. show wherein said second pad comprises an electroplated

90. The structure of Claim 83, Hayashida et al. show wherein said second has a thickness greater than 1 micron.

91. The structure of Claim 83, Hayashida et al. further comprising a wire formed by a wirebonding process and connected to said first chip.

92. The structure of Claim 83, Hayashida et al. show wherein said tin-containing material further comprises lead.

93. The structure of Claim 83, Hayashida et al. show wherein said tin-containing material further comprises silver.

94. Matsuo et al. (figures 1 to 19) specifically figures 1 and 12 show a multi-chip structure, comprising: a first chip **1,303** comprising: a semiconductor substrate **10** comprising multiple MOS devices, an interconnection layer **14** over said semiconductor substrate, a first pad **12c** over said semiconductor substrate, a passivation layer **15** over said interconnection layer, an opening in said passivation layer exposing said first pad, a trace **18** over said passivation layer, and a second pad **18,20** over said passivation layer, wherein said second pad is connected to said first pad through said trace and has a position different from that of said first pad from a top view; a second chip over said first chip; and a bump **21** connecting said second pad to said second chip.

95. The structure of Claim 94, Hayashida et al. show wherein said bump comprises copper.

96. The structure of Claim 94, Hayashida et al. show wherein said bump comprises nickel.

97. The structure of Claim 94, Hayashida et al. show wherein said bump comprises gold.

98. The structure of Claim 94, Hayashida et al. show wherein said bump comprises tin.

99. The structure of Claim 94, Hayashida et al. show wherein said bump comprises lead.

100. The structure of Claim 94, Hayashida et al. show wherein said bump comprises silver.

101. The structure of Claim 94, Hayashida et al. further comprising a wire formed by a wirebonding process and connected to said first chip.

Claims 75 to 82 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shibata (U.S. Patent # 6,734,556 B2).

75. Shibata (figures 1 to 17) specifically figures 1A and 16 show a multi-chip structure comprising: a first chip **1**; a second chip **2**; a conductive pillar **21,11** on the first chip, wherein said conductive pillar has a height greater than 3 microns; and a tin-containing material **22** connecting said conductive pillar to said second chip.

76. The structure of Claim 75, Shibata show wherein said conductive pillar comprises copper.

77. The structure of Claim 75, Shibata show wherein said conductive pillar comprises nickel.

78. The structure of Claim 75, Shibata show wherein said conductive pillar comprises gold.

79. The structure of Claim 75, Shibata show wherein said conductive pillar comprises tin.

80. The structure of Claim 75, Shibata further comprising a wire formed by a wirebonding process and connected to said first chip.

81. The structure of Claim 75, Shibata show wherein said tin-containing material further comprises lead.

82. The structure of Claim 75, Shibata show wherein said tin-containing material further comprises silver.

[0032] Also, it is preferable that the metals are made of Au and the low-melting point metal layer is made of Sn or an Au--Sn alloy and also the first semiconductor chip or substrate and the second semiconductor chip are superposed one on the other with the electrode terminals or the wirings thereof as facing each other and heated to a temperature at which the Au--Sn alloy or Sn melts, to be self-aligned and joined with each other. That is, when these portion can be joined to each other by use of the Au--Sn alloy and heating them to a temperature of 280.degree. C. or so, they melt completely and, therefore, needs no pressure application nor complete alignment, to be brought up by surface tension to the joining position such as the bump in self-alignment.

[0052] In the example shown in FIGS. 1, on both of the first and second semiconductor chips 1 and 2, the respective bump electrodes 11 and 21 are formed by plating etc. to a thickness of 10-30 .mu.m or so, in addition to which the bump electrode 11 of the first semiconductor chip 1 is provided with Sn (second metal) formed thereon to a thickness of 0.5-3.0 .mu.m by electroless plating or sputtering. The bump electrodes 11 and 21 themselves are formed conventionally in that, as shown in FIG. 1C illustrating the expanded cross-sectional view of the bump electrode, on the electrode terminals 12 and 22 made of aluminum are respectively formed barrier metal layer 14 and 24 in a two-layer or three-layer construction, for example, which consists of a first layer made of Ti or Cr, a second layer made of W, Pt, Ag, Cu, or Ni, and a third layer made of Au etc. Thereon are formed the bump electrodes 11 and 21 made of Au, Cu, etc. respectively. Note here that reference numerals 17 and 27 indicate an insulator film.

[0053] An Sn coating 11a is provided on the bump electrode 11 made of Au, so that at around a temperature of 230.degree. C., Sn with a melting point of 232.degree. C. or so melts to be alloyed with Au having a melting point of 1064.degree. C. to thereby provide an eutectic alloy and, at around a temperature of 280.degree. C., an alloy layer 3 made of an Au--Sn alloy is formed on the joining surface to permit both the bump electrode 11 and 21 to be melt-adhered to each other. (In case of bonding Au bump and Au bump, they are melt-adhered to each other when

heated to a temperature of 450.degree. C. or so under pressure because they are of the same metal.) That is, these bump electrodes 11 and 21 can be melt-adhered to each other at such a low temperature as not to damage the circuit elements formed on the semiconductor substrate. Therefore, any other metal than Au and Sn can be used as far as such a relationship is satisfied between the first metal making up the bump electrode 11 and the overlying second metal coating 11a that the second metal may have a lower melting point than the first metal and, therefore, the second metal can melt to thereby be alloyed with the first metal for melt-adhesion.

[0055] In the second semiconductor chip 2, on the other hand, for example, memory circuits are formed in a matrix, in such a configuration that portions connected to the driver circuit or the external lead are formed as the electrode terminal 22 on the surface of its semiconductor substrate, on the surface of which electrode terminal 22 is also formed the bump electrode 21 made of Au like in the case of the first semiconductor chip 1. This bump electrode 21 may have, if desired, an Sn coating formed thereon like in the case of the first semiconductor chip 1. Alternatively, the first semiconductor chip 1 has no Sn coating formed thereon, while the second semiconductor chip 2 may has an Sn coating formed only on the bump electrode 21. That is, it is only necessary to provide the Sn coating on at least one of these two chips.

[0057] To interconnect the bump electrodes 11 and 21 of the respective first and second semiconductor chips 1 and 2, for example, the first semiconductor chip 1 is put on a substrate stage which can be heated to then superpose the second semiconductor chip 2 thereon by a mounter in rough alignment of the bumps, which is heated to a temperature of 300.degree. C. or so while applying thereon load of around its own weight of the second semiconductor chip so that the Sn coating 11a may melt to form an eutectic with Au of the bump electrodes 11 and 21, thus forming the alloy layer 3. In this case, even if, as shown in FIG. 13A, the first and second semiconductor chips 1 and 2 are not completely aligned with each other, when the alloy layer 3 is formed at around a temperature of 300.degree. C. to melt this alloy layer, the second chip 2 moves, as shown in FIG. 13B, by surface tension of the alloy layer 3 in such a manner that they may be joined center-to-center of bump electrodes 11 and 21 each other (self-alignment).

When they are cooled then, the alloy layer 3 is solidified so that they may be adhered to each other.

[0058] This self-alignment is possible not only between one semiconductor chip and another but also between a substrate and a semiconductor chip as well, in which case low-melting point metal such as the Au--Sn alloy layer is melted. Note here that although this example has employed as the load only its own weight of the second semiconductor chip during joining, an extra some weight may preferably be added when the number of the joining portions such as bumps is large to thereby reduce the load for each of them. For example, load of 2 gram for each bump may be applied at a temperature of 350.degree. C. in joining.

[0070] Since Au diffuses almost 10 times as much as Sn, the Sn concentration over the bump electrodes 11 and 21 and the joining portion 3 after joining is distributed, as shown in FIG. 5, highest at the center of the joining portion where the Sn coating 11a is provided and lower gradually toward the root of the bump electrodes 11 and 21. Therefore, preferably the Sn coating thickness and the joining time and temperature are adjusted so that the Au concentration is at least 65 weight-percent even at the point where the Sn concentration hits the peak and 100 weight-percent at the root of the bump electrodes 11 and 21. Note here that the Au concentration is meant to be, for example, at least 65 weight-percent not all over the bump electrode surfaces but just over at least 60% of the whole area because the electrodes are not in a complete steady state. The joining time and temperature and the Sn layer thickness can be adjusted so that, for example, the Au concentration is at least 65 weight-percent at such a joining portion, still leaving a point where the Au concentration is 100 weight-percent.

[0071] More preferably, the Au--Sn eutectic layer (joining portion 3) is at least 0.8 .mu.m and 5.mu. or less in thickness. To this end, the Sn coating must be 0.1 to 4.0 .mu.m in thickness. In this case, to leave a complete Au layer as is, the Au layer (bump electrode) must be formed thick.

[0072] Although the example shown in FIGS. 1A to 1C has the bump electrodes 11 and 21 formed on the electrode terminals of the first and second semiconductor chips 1 and 2 respectively, the bump electrode only needs to be formed on at least one of these electrode terminals as far as it is positioned at the

interconnection or may be joined to the electrode terminal. This case is exemplified in FIG. 6, which shows an expanded cross-sectional view of only the interconnection. That is, on the connection electrode terminal 12 of the first semiconductor chip 1, instead of a bump electrode, a metal film (Au film) 15 made of, for example, Au with a thickness of 0.2 to 0.5 .mu.m is provided via the barrier metal layer 14, on which a second metal coating (Sn coating) 16 is provided to the same thickness as the Au film 15. On the second semiconductor chip 2, on the other hand, the bump electrode 21 made of Au is formed in almost the same manner as above, in such a construction that the bump electrode 21 is alloyed with the Sn coating 16 to thereby be melt-adhered to the Au film 15 overlying the electrode terminal 12. This Sn coating 16 may be provided on the side of the bump electrode 21 of the second semiconductor chip 2 or on both sides and connected with them in the same way as the above.

[0082] Although the above-mentioned examples have joined the interconnection portions to each other via the bumps by joining and alloying the first metal with a relatively high melting point and the second metal with a relatively low melting point with each other, such third metal such as, for example, an Au--Sn alloy that melts at a temperature of 300.degree. C. or so can be provided on that joining surface and then melted for joining. This is exemplified in FIG. 12, which shows, like FIG. 6, only the bump electrode as expanded. The third metal may be an Au--Sn alloy etc. described later.

[0083] In FIG. 12, the same components with FIG. 1 are indicated by the same reference numerals and their explanation is omitted. The bump electrode 11 provided on the barrier metal layer 14 of the first semiconductor chip 1 is made of, for example, Ni and has at the joining portion on its right surface a low-melting point alloy layer such as an Au--Sn eutectic alloy (with a ratio of, e.g., Au:Sn=80:20) as a third metal layer 19 formed to a thickness of, for example, 0.5 to 3.0 .mu.m or so. This Au--Sn layer 19 is formed to such a thickness by sputtering, electroless plating, etc.

[0084] The semiconductor chip 1 provided with the Au--Sn layer 19 on the bump electrode 11 can be joined with the second semiconductor chip 2 by, like in the case of the above-mentioned example shown in FIGS. 1A and 1B, putting the first semiconductor device 1 on, for example, a board stage which can be heated and aligning it with the second semiconductor chip 2

superposing the second semiconductor chip 2 thereon with a mounter in such a manner as to align their respective bumps with each other and then heating them to a temperature of 300.degree. C. or so under pressure so that the Au--Sn alloy layer 19 may melt and diffuse into Ni of the bump electrodes 11 and 21 to thereby form an intermetallic compound for so-called diffusive joining. Note here that as mentioned above, in an Au--Sn alloy, Au is at least 10 times as large as Sn in diffusion coefficient.

[0085] In this construction, since the bump electrode surface and the Au--Sn alloy layer are intermetallic bonded with each other, they are securely joined to each other at a solder reflow temperature of 260.degree. C. or so during the assembling of the semiconductor device. At the central portion, on the other hand, the Au--Sn alloy layer in an Au--Sn alloyed state and, therefore, melts near a temperature of 300.degree. C. or so but is small in layer thickness, so that it is not peeled off during solder reflowing because it is in the packaged semiconductor device unless an external force is applied on the semiconductor chips. If an external force is applied on it at a high temperature of 300.degree. C. or so, the low-melting point alloy layer melts and, therefore, can be peeled off easily. As such, for example, to replace the second semiconductor chip with a new one, by heating it nearly to a temperature of 280-300.degree. C. and applying an external force thereon, it can be easily separated, thus giving a merit of easy replacement of the semiconductor chip. Note here that the thickness of the Au--Sn alloy layer can be adjusted so that it may not easily peeled off at around a temperature of 300.degree. C.

[0084] The semiconductor chip 1 provided with the Au--Sn layer 19 on the bump electrode 11 can be joined with the second semiconductor chip 2 by, like in the case of the above-mentioned example shown in FIGS. 1A and 1B, putting the first semiconductor device 1 on, for example, a board stage which can be heated and aligning it with the second semiconductor chip 2 superposing the second semiconductor chip 2 thereon with a mounter in such a manner as to align their respective bumps with each other and then heating them to a temperature of 300.degree. C. or so under pressure so that the Au--Sn alloy layer 19 may melt and diffuse into Ni of the bump electrodes 11 and 21 to thereby form an intermetallic compound for so-called diffusive joining. Note here that as mentioned above, in an Au--Sn alloy, Au is at least 10 times as large as Sn in diffusion coefficient.

Claims 91 and 101, **insofar as claim 101 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuo et al. (U.S. Patent # 6,787,442 B2) in view of Shibata et al. (U.S. Patent # 6,734,556 B2).

Matsuo et al. show the features of the claimed invention as detailed above, but fail to explicitly show a wire formed by a wirebonding process and connected to said first chip.

Shibata et al. is cited for showing a chip on chip semiconductor device. Specifically, Shibata et al. (figure 3) discloses a wire formed by a wirebonding process and connected to said first chip for the purpose of providing a semiconductor device having a construction which is capable of securely interconnecting a parent chip and a child chip and separating from each other easily without affecting elements in the semiconductor chips when child chip is removed.

Therefore, it would have been obvious to one of ordinary skill in the art to use Shibata et al.'s wirebonding process connected to the first chip to modify Matsuo et al.'s chip structure for the purpose of providing a semiconductor device having a construction which is capable of securely interconnecting a parent chip and a child chip and separating from each other easily without affecting elements in the semiconductor chips when child chip is removed.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,686,685,723,724,728,676,784,786,775,776,758,760,737,734,738	12/10/05
Other Documentation: foreign patents and literature in 257/777,686,685,723,724,728,676,784,786,775,776,758,760,737,734,738	12/10/05
Electronic data base(s): U.S. Patents EAST	12/10/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Art Unit 2826

AOW
12/10/05